IFW

Docket Number: 011765-0304367
Client Reference: AF/JG/P9094US

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of

FLORIN UDREA

Group Art Unit: 2814

Application No.: 10/602,065

Examiner: PHAM, Hoai V.

Filed: June 24, 2003

Confirmation No.: 1160

For: LATERAL SEMICONDUCTOR DEVICE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR 1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom. Applicants respectfully request the Examiner return an initialed copy of the enclosed Form PTO-1449 to Applicants with the next Office communication to indicate that the reference(s) has been considered, per MPEP § 609.

This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of the Notice of Allowance, but before payment of the Issue Fee. Please charge Deposit Account 03-3975, under order number 011765-0304367, in the amount of $180.00 in payment of the fee under 37 CFR 1.17(i)(p). Please credit or debit Deposit Account 03-3975 as needed to ensure consideration of the disclosed information.

These references are being cited with respect to an International Search Report which was issued for International Application No. PCT/GB 03/02635. Applicant is submitting U.S. Patent No. 2002/0096708 as the U.S. equivalent of EP 1 213 768.

12/01/2004 EABUBAK1 00000009 033975 10602065
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Respectfully Submitted,

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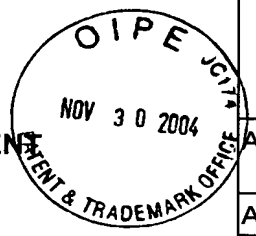
FORM PTO-1449 (modified)
To: U.S. Department of Commerce
(PW FORM PAT-1449)
Patent and Trademark Office



Atty. Dkt. No.	M#	
	304367	AF/JG/P9094US

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Applicant: Florin UDREA

Appln. No.: 10/602,065

Filing Date: June 24, 2003

Date: November 30, 2004 Page 1 of 1 Examiner: Pham, Hoai V. Group Art Unit: 2814

U.S. PATENT DOCUMENTS

Examiner's Initials*		Document Number	Date MM/YYYY	Name (Family Name of First Inventor)	Class	Sub Class	Filing Date (if appropriate)
	AR	2002/0096708 A1	07/2002	Ahlers et al.			
	BR						
	CR						
	DR						
	ER						
	FR						
	GR						
	HR						
	IR						
	JR						

FOREIGN PATENT DOCUMENTS

		Document Number	Date MM/YYYY	Country	Inventor Name		English Abstract		Translation Readily Available	
							Enclosed	No	Enclose	No
	KR	1 026 750 A1	08/2000	EUROPE	Udrea					
	LR	WO 00/35023	06/2000	PCT	LetaVic					
	MR	2 380 056	03/2003	GREAT BRITAIN	Amaratunga et al.					
	NR									
	OR									
	PR									
	QR									
	RR									

OTHER (Including in this order Author, Title, Periodical Name, Date, Pertinent Pages, etc.)

	SR	Ng, R., et al., "Lateral Unbalanced Super Junction (USJ)/3D-RESURF for High Breakdown Voltage on SOI," 4 June 2001, pgs. 395-398.
	TR	Udrea, F., et al., "Lateral Insulated Gate Bipolar Transistor (LIGBT) Structure Based on Partial Isolation SOI Technology," 8 May 1997, pgs. 907-909.
	UR	Chen, X.B., et al., "Lateral High-Voltage Devices Using an Optimized Variational Lateral Doping," Int. J. Electronics, 1996, Vol. 80, No. 3, pgs. 449-459.
	VR	Amberetu, M., et al., "150-V Class Superjunction Power LDMOS Transistor Switch on SOI, 4 June 2002, pgs. 101-104.
	WR	
	XR	
	YR	

Examiner Date Considered:

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.